

A Novel Circuit Configuration of UPS with Auxiliary Inverter and Its Specific Control Implementations

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ABSTRACT

The rapid expansion of small computers over the last 10-odd years has brought about great changes in the circumstances affecting UPSs. There are strong demands that UPSs become much smaller and lighter, and more economical, which has resulted in the wide application of the circuit topology without transformer. A disadvantage of such UPS topology is that the DC link voltage is very high, which invites decreased reliability and increased cost of battery bank. Some circuit configurations were proposed to eliminate this disadvantage, but they still had problems. In this paper, a novel circuit configuration which eliminates these problems is proposed and evaluated by the experimental results of prototype UPS.

Keywords: UPS, Without transformer, Half-bridge Inverter, PFC converter

1. Introduction

Nowadays, rapid growth in the use of computers and its systems has brought great changes to the circumstances of UPS (Uninterruptible Power Supply). Although UPS was originally a typical kind of industrial electrical equipment, in the last few years they are increasingly used as a peripheral device for small computers. For that reason, UPS has been strongly demanded to become smaller, lighter, and more economical. To be economical, UPS must not only be cheaper but also have high efficiency.

Major changes have come about in UPS circuit topologies in response to these demands. Over the last 10-odd years the dominant circuit configurations in on-line UPSs have changed from the topology with

low-frequency transformer to with high-frequency transformer and to without transformer^{[1][2]}. These changes led to substantially better UPS economy, and also made them far smaller and lighter^{[3][4]}. Nowadays the topologies without transformer are most popular for on-line UPS^{[5][6]}. In this paper a novel on-line UPS topology without transformer and its specific control strategy are presented and evaluated on the basis of experimental results.

2. Conventional Circuit Configuration

Fig. 1 shows the basic circuit configuration of the UPS without transformer. It combines a half-bridge, PFC (Power Factor Correction) converter composed of T1, T2 and L1, and a half-bridge inverter comprising T3, T4, and L2^{[7][8]}. In this configuration, the input S phase and the output V phase have the same potential, which makes it possible to eliminate the transformer because the voltage potential of load is stable^[9].

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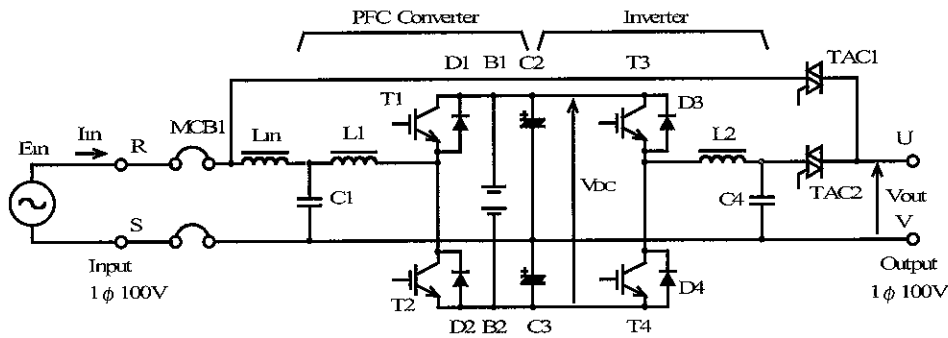


Fig 1 Basic circuit configuration of on-line UPS without transformer

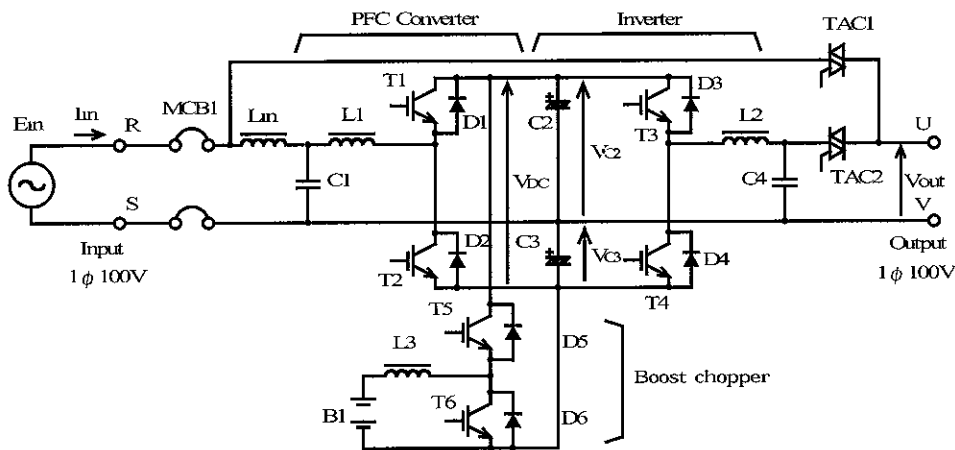


Fig 2 Conventional circuit configuration of on-line UPS with boost chopper

Because the circuit configuration of Fig. 1 needs no transformer, it is not only much smaller, lighter, and more economical, it is also easy to achieve high efficiency. But because this circuit topology employs a half-bridge inverter, it needs a high voltage of about 340 V for DC link voltage V_{DC} in order to obtain the output voltage of 100V. This necessitates connecting a very large number of small capacity battery cells in series, which invites decreased reliability and increased cost.

Fig 2 shows the circuit topology which is proposed by the authors previously to overcome these problems^[9]. To the basic circuit in Fig 1 it adds a chopper circuit comprising T5, T6, and L3, which boosts the voltage of battery B1 and supplies it to DC link voltage V_{DC} . This makes it possible to keep battery voltage low, thereby ensuring the reliability and low cost of the battery B1. However, this circuit topology requires the addition of two

switching elements and the inductor L3, which made it less economical especially because inductor is expensive. Additionally, chopper circuit has no capability to balance the high-voltage side (V_{C2}) and low-voltage side (V_{C3}) of its output voltage. For example, if a half-wave rectification circuit is connected to the load, the unbalance between V_{C2} and V_{C3} will increase and prevent the generation of a normal output voltage of inverter.

3. Proposed Circuit Configuration

In order to improve the problem mentioned above, a novel circuit configuration with an auxiliary inverter shown in Fig 3 is proposed. Battery bank is connected to the AC input side through a simple auxiliary inverter which operates at a commercial frequency.

When receiving commercial power, T5-T8 are off and battery bank B1 is disconnected from the UPS circuit. When a power failure is detected, TAC1 is instantaneously turned off and the UPS circuit is disconnected from the commercial power grid. At the same time, auxiliary inverter starts the operation.

T5 and T8 turn on and off simultaneously. T6 and T7 are also switched simultaneously. T5/T8 and T6/T7 are turned on and off alternately. As a result, battery voltage is changed to the square-wave AC voltage of the commercial power frequency and supplied to the PFC converter circuit, which receives this square-wave AC voltage and continues the operation in the same way as when using commercial power.

In this circuit configuration, the voltage of battery bank is boosted by the PFC converter and supplied to the inverter. It means that the battery bank with low voltage can provide the power to the inverter which needs the high input voltage of 340V. The battery bank whose rated voltage is 96V have been adopted to the 1kVA UPS prototype.

PFC converter has two active switches of T1 and T2. By controlling the duty ratio of T1 and T2 respectively, PFC converter output voltage VC2 and VC3 are controlled individually. It means that the proposed circuit configuration can keep the voltage balance of VC2 and VC3, and overcomes the disadvantage of conventional circuit.

4. Control Implementation of the PFC Converter

The PFC converter circuit shown in Fig 3 is regulated through the current-mode control circuit shown in Fig 4 so as to obtain an unity power factor and a sinewave line current shaping effects. The current of reactor L1 is compared to a reference wave of the same phase as commercial power, and amplified. Its error signal V_{er} is modulated with a 40 kHz triangular wave, and the PWM signal that drives transistors T1 and T2 is obtained. In this way, the current wave form of reactor L1 becomes equal to the reference wave. Input current of PFC converter has the same phase as AC input voltage and a sinusoidal waveform with no distortion, because reference wave is a sinewave. The offset voltage of the reference wave is controlled so as to keep the voltage balance of VC2 and VC3.

The control circuit operates in the same manner whether commercial power is available or not, so even though the input voltage waveform of the PFC converter is square, its input current waveform is a sinusoidal. With the minimum AC input voltage of 90V, the input current of the UPS is 10.6 Arms which means 15.0 A peak. At power failure, as mentioned above, input power of the PFC converter is supplied by the battery bank through the auxiliary inverter. Battery bank consists of 48 cells of lead acid batteries and the rated voltage of the battery bank is 96V and

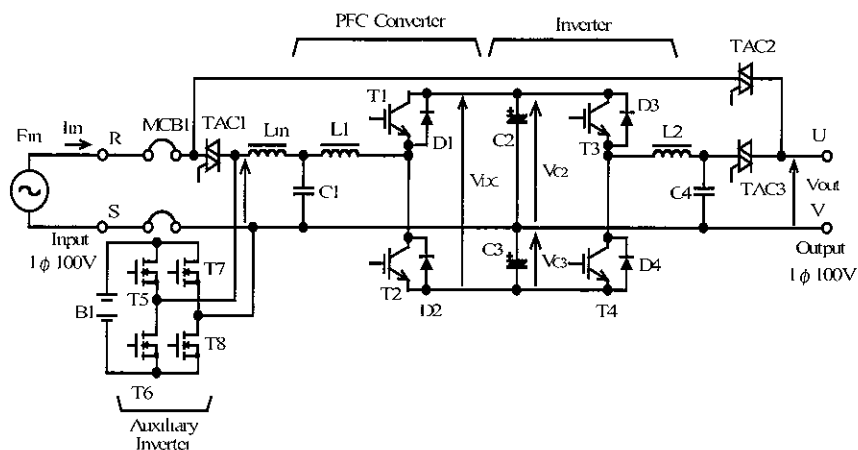


Fig 3 Proposed circuit configuration of on-line UPS with auxiliary inverter

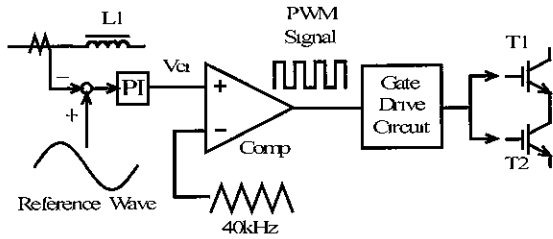


Fig 4 Control circuit block diagram of PFC converter

minimum voltage is 77V at the end of discharge period. Consequently, the maximum input current of the PFC converter at power failure is calculated to be 12.4A by the following formula

$$\begin{aligned} \text{Maximum input current} \\ = 10.6 \text{ Arms} \times 90\text{V} - 77\text{V} = 12.4 \text{ Arms} \end{aligned}$$

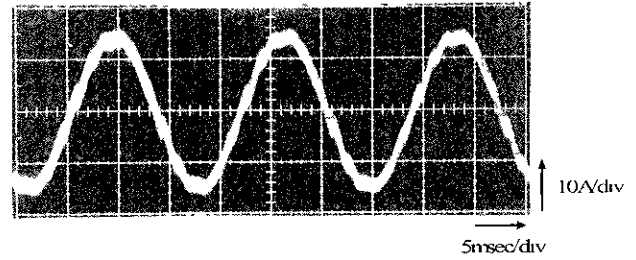
The peak value of 12.4Arms is 17.5Apeak. It means that the peak current of the inductor L1 at power failure is about 17% larger than that in normal operation and it brings the increase of size and cost of inductor L1.

Because input current waveform must be shaped to be sinusoidal in normal operation, the current waveform of L1 must be changed into a sinusoidal waveform, but this restriction does not apply during power failure. The authors therefore developed a new control strategy in which, at power failure, the peak value of L1 current is suppressed by changing the reference wave provided by the microcomputer circuit into a trapezoidal wave as shown in Fig 5. The trapezoidal reference wave brings the trapezoidal current to L1 and the peak current of L1 is reduced to the value of 14.5A which is small enough to prevent the increase of size and cost of inductor L1.

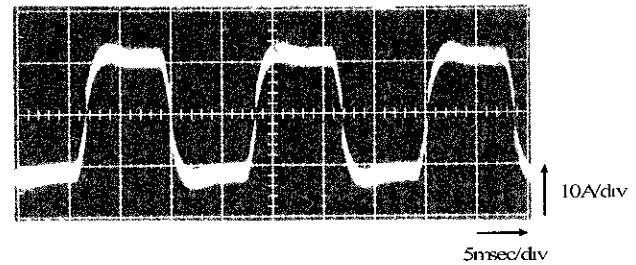
Fig 6 shows the current waveforms of inductor L1. It is shaped to the sinusoidal wave in normal operation and trapezoidal wave at power failure.

	Wave Form
In Normal Operation	
At Power Failure	

Fig 5 Reference Wave of Control Circuit of PFC Converter



(a) In normal operation



(b) At power failure

Fig 6 Current waveforms of inductor L1

5. General Description of the 1kVA UPS Prototype

1kVA UPS prototype incorporating the auxiliary inverter shown in Fig 3 is developed. Fig. 7 shows the waveforms of the input voltage and input current of the developed 1kVA UPS. Input current is undistorted sine wave of the same phase as input voltage. Fig 8 shows the output voltage and output current waveforms with a rectifier load. As the figure shows, even if the current waveform is distorted with a large crest factor, the output voltage is a sine wave with little distortion.

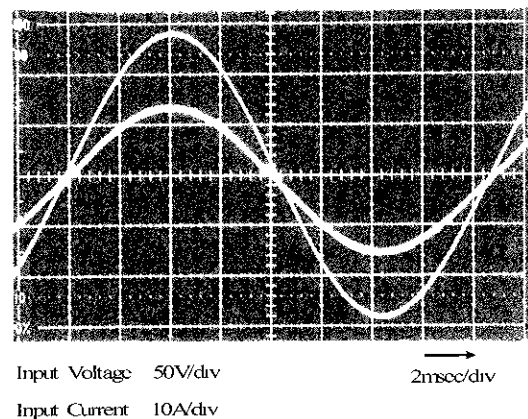


Fig 7 Waveforms of input voltage and current at rated input and output

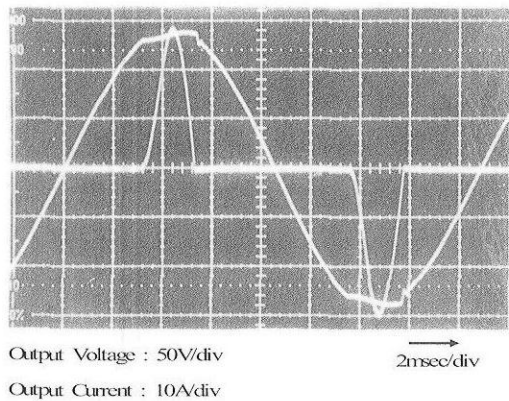


Fig. 8. Waveforms of output voltage and current at rectification load.

Table 1 shows the characteristics of the UPS. As shown in Fig. 7, input current is sine wave of the same phase as input voltage, so the input power factor is 99%, and input current distortion is 3%. Output voltage distortion is under 5% even with a rectifier load (non linear load). Because of the high efficiencies of 84.2% with the 1kVA UPS, a small cooling fan is sufficient, and acoustic noise is less than 40 phons.

Fig. 9 shows the photograph of the UPS. It is small and light: the volume and weight of the 1kVA UPS is 21.9 liters and 24 kg.

Table 1. Characteristics of the 1kVA UPS prototype.

Items	Characteristics
Input Voltage	1 ϕ 100V 50/60Hz
Input Power Factor	99%(at full load)
AC Input Current THD	3%(at full load)
Output Capacity	1kVA 800W
Output Voltage	1 ϕ 100V 50/60Hz
Voltage Accuracy	within $\pm 2\%$
Frequency Accuracy	within $\pm 0.5\%$
Output Voltage Distortion	1.8% (at linear load) 4.0% (at non linear load)*
AC/AC Efficiency	84.2% (at full load)
DC/AC Efficiency	82.2% (at full load)
Battery Type	Sealed Lead-Acid
Back up Time	7 minutes
Audible Noise	less than 40 dB
Dimensions	330W 190H 350L
Weight	24kg

* Full bridge rectification circuit with large smoothing capacitor is used for non linear load.

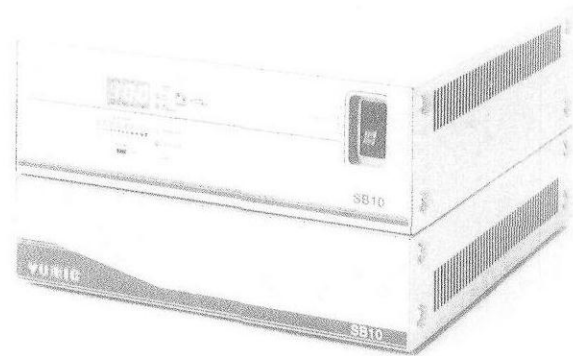


Fig. 9. Exterior overview of 1kVA UPS prototype.

6. Conclusion

The state-of-the art UPS incorporating simple half-bridge PFC converter and half-bridge PWM inverter circuits with no electrical isolation power stage has attracted special interest recently. However, this attractive UPS topology has significant disadvantage that storage batteries have to be connected to the high voltage DC link bus. The authors were able to overcome this shortcoming without any substantial cost increase by employing the circuit of auxiliary inverter. The 1kVA UPS prototype developed using the circuit configurations made it possible to achieve excellent performance including small size, light weight, high efficiency, high power factor and low distortion.

References

- [1] K. Hirachi and A. Ueda, "Overview of power factor correction converter for uninterruptible power supply", Proceedings of the 1999 Japan Industry Applications Society Conference, Vol. 1, pp. 75-78, 1999.
- [2] M. Yatsu, "State-of-the-art of uninterruptible power systems", Proceedings of the 1999 Japan Industry Applications Society Conference, Vol. 2, pp. 25-28, 1999.
- [3] Y. Yamakata, M. Yatsu, E. Iwabuchi, and K. Yoda, "Development of new series mini-UPS", Tran. of Japan Society for Power Electronics, Vol. 25, No. 1, pp. 81-89, 1999.
- [4] H. Daishoji and T. Yamamoto, "Compact uninterruptible power system type SHU102", Sanken technical journal, Vol. 27, No. 1, pp. 11-18, 1995.

- [5] Y. Uematsu, T. Ikeda, N. Hirao, S. Totsuka, T. Ninomiya, and H. Kawamoto, "A study of the high performance single phase UPS" Proceedings of IEEE Power Electronics Specialists Conference (PESC), pp. 872-1878, 1998.
- [6] A. Kanouda, Y. Sakurai, K. Kubo, K. Shimada, H. Kunisada, and metsu, "All digital controlled three-phase UPS without inverter-transformer", Proceedings of IEEJ/IEEE Joint IAS Power Conversion Conference (PCC), pp. 991-996, 1997.
- [7] C. Chen and D.M. Divan, "Simple topologies for single phase AC line conditioning", IEEE Trans. on Industry Applications, Vol. 30, No. 2, pp. 406-412, 1994.
- [8] W.J. Ho, M.S. Lin, and W.S. Feng, "Common-neutral-type AC/DC/AC topologies with PFC pre-regulator", Proceedings of IEEE International Conference on Power Electronics and Drive Systems (PEDS), pp. 53-58, 1997.
- [9] Katsuya Hirachi and Mutsuo Nakaoka, "Feasible high-performance uninterruptible power supply incorporating current-mode controlled two-quadrant chopper-fed battery link", International Journal of Electronics, Vol. 87, pp. 1341-1351, 2000.

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